UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/697,354 | 10/29/2003 | Brian Harold Kelley | 030621 | 7523 |

23696 7590 08/24/2006

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

| EXAMINER | |
|---|---|
| MCKAY, KERRY A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2131 | |

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/697,354 | KELLEY ET AL. | |
| | Examiner | Art Unit | |
| | Kerry McKay | 2131 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/7/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This is a final action in response to communications filed June 7, 2006. Claims 1-19 were originally filed. New claims 20-26 have been entered. Claims 1-26 are pending in this action.

### *Drawings*

2. The drawings were received on June 7, 2006. These drawings are acceptable.

### *Response to Arguments*

3. Applicant's arguments filed June 7, 2006 have been fully considered but they are not persuasive.

4. Applicant argues on page 10 that Freeman et al. does not disclose or suggest operating in two modes. Examiner respectfully disagrees. The non-secure mode of Freeman et al., depicted as item 209 in figure 2, is itself the combination of two privilege levels. Specifically, it provides the execution of instructions and execution of ICE commands.

### *Claim Objections*

5. Claim 21 is objected to because of the following informalities: the phrase "... determining further comprising ..." is awkward. Examiner believes that Applicant

intended "... ***the step of*** determining further comprising ..." or "... determining further comprise***s***..."

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-21 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Freeman et al., US Patent 6,925,570 B2. Examiner notes that corresponding prior art terms may accompany the claim language in bracketed form.

7. Regarding claim 1, Freeman et al. teach a method for selectively enabling operating modes of a device during a device initialization, wherein the operating modes comprise a privileged mode and a non-privileged mode, and the method comprising:
determining during the device initialization whether the device is to operate in the privileged mode or in both the privileged and non-privileged modes (figure 2, step 208, column 4, lines 62-63);
enabling the privileged mode if it is determined that the device is to operate only in the privileged mode (figure 2, step 207, column 5, lines 1-2); and

enabling both the privileged and the non-privileged modes if it is determined that the device is to operate in both the privileged and the non-privileged modes (figure 2, step 209, column 4, lines 64-66).

8. Regarding claim 6, Freeman et al. teach an apparatus for selectively enabling operating modes of a device during a device initialization, wherein the operating modes comprise a privileged mode and a non-privileged mode, and the apparatus comprising:
a flag (s-latch) (figure 1, item 107, column 3, lines 36-42); and
selection logic that operates to read the flag (s-latch) to set the operating mode of the device, wherein if the flag is set the selection logic enables the privileged mode, and if the flag is not set, the selection logic enables both the privileged and non-privileged modes (figure 2, steps 207-209, column 4, line 62 – column 5, line 2).

9. Regarding claim 10, Freeman et al. teach an apparatus for selectively enabling operating modes of a device during a device initialization, wherein the operating modes comprise a privileged mode and a non-privileged mode, and the apparatus comprising:
means for determining during the device initialization whether the device is to operate in the privileged mode or in both the privileged and non-privileged modes (figure 2, step 208, column 4, lines 62-63);
means for enabling only the privileged mode if it is determined that the device is to operate only in the privileged mode (figure 2, step 207, column 5, lines 1-2); and

means for enabling both the privileged and the non-privileged modes if it is determined that the device is to operate in both the privileged and the non-privileged modes (figure 2, step 209, column 4, lines 64-66).

10. Regarding claim 15, Freeman et al. teach a computer-readable media comprising instructions, which when executed by a processor in a device, operate to selectively enable operating modes of a device during a device initialization, wherein the operating modes comprise a privileged mode and a non-privileged mode, and the computer-readable media comprising:

instructions for determining during the device initialization whether the device is to operate in the privileged mode or in both the privileged and non-privileged modes (figure 2, steps 207-209, column 4, line 62 – column 5, line 2);

instructions for enabling only the privileged mode if it is determined that the device is to operate only in the privileged mode (figure 2, step 207, column 5, lines 1-2); and

instructions for enabling both the privileged and the non-privileged modes if it is determined that the device is to operate in both the privileged and the non-privileged modes (figure 2, step 209, column 4, lines 64-66).

11. As per claim 20, Freeman et al. teach a method for selectively enabling operating modes of a device, comprising:

determining during the device initialization whether the device is to operate in at least one of a privileged mode and a combined privileged and non-privileged mode (figure 2, step 208, column 4, lines 62-63); and

enabling the combined privileged and non-privilege mode for each determination that the device is to operate in the combined privileged and non-privileged mode (figure 2, step 209, column 4, lines 64-66).

12. Regarding claim 24, Freeman et al. teach an apparatus, comprising:

a selectable one of a plurality of operating modes, the plurality of operating modes comprising at least a privileged operating mode and a combined privileged and non-privileged operating mode (figure 2, steps 207 and 209, column 4, lines 22-38);

a memory comprising a flag having at least two settings, wherein one predetermined setting of the at least two settings corresponds to the combined privileged and non-privileged operating mode (column 4, line 54 – column 5, line 2); and

selection logic communicatively coupled with the memory and operable to read the flag to set an operating mode of the apparatus, wherein the selection logic is operable to enable the combined privileged and non-privileged mode on the apparatus based on reading the one predetermined setting of the at least two settings (figure 2, steps 208 and 209, column 4, line 63 – column 5, line 2).

13. As per claim 2, the method of Freeman et al. teaches the method of claim 1, wherein the step of determining comprises testing a flag (s-latch) (figure 2, step 208, column 4, lines 62-63).

14. As per claim 3, the method of Freeman et al. teaches the method of claim 1, wherein the step of enabling only the privileged mode comprises controlling one or more device memory management units to enable only the privileged mode (column 1, lines 19-29, column 3, lines 43-46, column 5, lines 1-2, where it is inherent that the processor contains a MMU to manage communications with memory).

15. As per claim 4, the method of Freeman et al. teaches the method of claim 1, wherein the step of enabling both the privileged mode and the non-privileged modes comprises controlling one or more device memory management units to enable both modes (column 1, lines 19-29, column 3, lines 43-46, column 4, lines 63-66, where it is inherent that the processor contains a MMU to manage communications with memory).

16. As per claim 5, the method of Freeman et al. teaches the method of claim 1, wherein the device is a wireless device (figure 3, column 5, lines 3-50, where the system may be realized as a laptop).

17. As per claim 7, the apparatus of Freeman et al. teaches the apparatus of claim 6, further comprising a memory that stores the flag (s-latch) (figure 2, step 208, column 4, lines 54-63, where NVRAM stores the data that sets the s-latch).

18. As per claim 8, the apparatus of Freeman et al. teaches the apparatus of claim 6, further comprising one or more memory management units that are controlled by the selection logic to set the operating mode of the device (column 1, lines 19-29, column 3, lines 43-46, column 4, line 62 – column 5, line 2, where it is inherent that the processor contains a MMU to manage communications with memory).

19. As per claim 9, the apparatus of Freeman et al. teaches the apparatus of claim 6, wherein the device is a wireless device (figure 3, column 5, lines 3-50, where the system may be realized as a laptop).

20. As per claim 11, the apparatus of Freeman et al. teaches the apparatus of claim 10, wherein the means for determining comprises means for testing a flag (s-latch) (figure 2, step 208, column 4, lines 62-63).

21. Regarding claim 12, the apparatus of Freeman et al. teaches the apparatus of claim 10, wherein the means for enabling the only privileged mode comprises means for controlling one or more device memory management units to enable only the privileged

mode (column 1, lines 19-29, column 3, lines 43-46, column 5, lines 1-2, where it is inherent that the processor contains a MMU to manage communications with memory).

22. As per claim 13, the apparatus of Freeman et al. teaches the apparatus of claim 10, wherein the means for enabling both the privileged mode and the non-privileged modes comprises means for controlling one or more device memory management units to enable both modes (column 1, lines 19-29, column 3, lines 43-46, column 4, lines 63-66, where it is inherent that the processor contains a MMU to manage communications with memory).

23. As per claim 14, the apparatus of Freeman et al. teaches the apparatus of claim 10, wherein the device is a wireless device (figure 3, column 5, lines 3-50, where the system may be realized as a laptop).

24. As per claim 16, the computer-readable media of Freeman et al. teaches the computer-readable media of claim 15, wherein the instructions for determining comprise instructions for testing a flag (s-latch) (figure 2, step 208, column 4, lines 62-63).

25. As per claim 17, the computer-readable media of Freeman et al. teaches the computer-readable media of claim 15, wherein the instructions for enabling the only privileged mode comprise instructions for controlling one or more device memory management units to enable only the privileged mode (column 1, lines 19-29, column 3,

lines 43-46, column 5, lines 1-2, where it is inherent that the processor contains a MMU to manage communications with memory).

26. As per claim 18, the computer–readable media of Freeman et al. teaches the computer-readable media of claim 15, wherein the instructions for enabling both the privileged mode and the non-privileged modes comprise instructions for controlling one or more device memory management units to enable both modes (column 1, lines 19-29, column 3, lines 43-46, column 4, lines 63-66, where it is inherent that the processor contains a MMU to manage communications with memory).

27. As per claim 19, the computer-readable media of Freeman et al. teaches the computer-readable media of claim 15, wherein the device is a wireless device (figure 3, column 5, lines 3-50, where the system may be realized as a laptop).

28. As per claim 21, the method of Freeman et al. teaches the method of claim 20, wherein determining further comprising reading a flag in a memory of a device, the flag having at least two settings, wherein one predetermined setting of the at least two settings corresponds to the combined privileged and non-privileged operating mode (figure 2, steps 203, 204, and 208, column 4, line 54 – column5, line 1, where NVRAM stores the data that sets the s-latch).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 22, 23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freeman et al., US Patent 6,925,570 B2, in view of McGrath et al., US Patent Application Publication 2004/0210764 A1.

30. Regarding claim 22, the method of Freeman et al. teaches the method of claim 20. The method of Freeman et al. does not teach partitioning memory.

McGrath et al. teach processors employing the x86 architecture, wherein memory is partitioned (isolated) into two privilege levels: kernel mode (CPL0, most privileged) and user mode (CPL3, least privileged) ([0005]-[0010]). It would have been obvious to one of ordinary skill in the art at the time of invention to partition the memory of Freeman et al. into the privilege levels of the x86 processor, namely kernel and user modes, because the x86 architecture protects applications from interfering with each other and was well known at the time of Applicant's invention.

31. As per claim 23, the method of Freeman et al. and McGrath et al. teaches the method of claim 22, wherein enabling further comprises restricting operation of the non-

privileged code to the non-privileged code region of the code memory and to the non-privileged data region of the data memory (McGrath et al., [0005]-[0009]).

32. As per claim 25, the apparatus of Freeman et al. teaches the apparatus of claim 24, wherein the memory is operable to store code and data (figures 1 and 3). The apparatus of Freeman et al. does not teach partitioning memory.

McGrath et al. teach processors employing the x86 architecture, wherein memory is partitioned (isolated) into two privilege levels: kernel mode (CPL0, most privileged) and user mode (CPL3, least privileged) ([0005]-[0010]). It would have been obvious to one of ordinary skill in the art at the time of invention to partition the memory of Freeman et al. into the privilege levels of the x86 processor, namely kernel and user modes, because the x86 architecture protects applications from interfering with each other and was well known at the time of Applicant's invention.

33. As per claim 26, the apparatus of Freeman et al. and McGrath et al. teaches the apparatus of claim 25, wherein the first memory management unit is operable to restrict operation of the non-privileged code to the non-privileged code region of the memory, and wherein the second memory management unit is operable to restrict operation of the non-privileged code to the non-privileged data region of the data memory (McGrath et al., [0005]-[0010]).

***Conclusion***

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kerry McKay whose telephone number is (571) 272-2651. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KM
8/15/06

CHRISTOPHER REVAK
PRIMARY EXAMINER

8/12/06